REMARKS

The present application was filed on February 20, 2002 with claims 1 through 20. Claims 1 through 20 are presently pending in the above-identified patent application.

In the Office Action, the Examiner rejected claims 1-20 under 35 U.S.C. 101 for being directed to non-statutory subject matter, and rejected claims 1-20 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner rejected claims 1-20 under 35 U.S.C. §102(e) as being anticipated by Chilimbi et al. (United States Patent Number 6,321,240 B1).

Section 101 Rejections

Claims 1-20 were rejected under 35 U.S.C. 101 for being directed to non-statutory subject matter. In particular, the Examiner asserts that, in claim 1, for example, the establishing of a bound based on said number of live frames does not provide a useful, concrete, and tangible result.

Applicants note that the present disclosure teaches that

> a critical parameter of a real-time task is its maximum response time over all possible inputs. In some systems, a task scheduler allocates a processor's cycles among multiple tasks to meet their response time requirements. *Thus, the worst-case execution time of each task must be known. When instruction timings or execution paths are uncertain, conservative (worst case) assumptions are often made that may* ***waste system capability or lead to an unnecessarily costly system.*** *If the resulting worst-case time-bound is loose, a task is allocated more execution time than it can possibly use,* ***wasting system capability and performance.*** Efficient system design thus requires methods to tightly estimate the effect of complex cache behavior. *A need therefore exists for methods and apparatus that evaluate the additional execution time of the primary, interrupted task attributed to any interrupts. A further need exists for methods and apparatus that establish a bound on the effect of task interference in an instruction cache shared by multiple tasks.*
> (Page 2, lines 1-12; emphasis added.)

The present disclosure also teaches that

> the present invention recognizes that the eviction of blocks from a live frame by an interrupt causes a future miss that would not otherwise occur and

> that evictions from live frames are the only evictions that cause misses that would not otherwise occur.
>
> The present invention thus *provides a more accurate estimate of the maximum additional execution time of a task that results from servicing an interrupt during its execution.*
>
> (Page 2, lines 20-24; emphasis added.)

Thus, the establishment of a bound on the execution time of an application due to task interference in a shared instruction cache, and the establishment of a bound based on the number of live frames are both useful, concrete, and tangible results for ***improving system performance.***

In any case, the Supreme Court has stated that the "[t]ransformation and reduction of an article 'to a different state or thing' is the clue to patentability of a process claim." *Gottshalk v. Benson*, 409 U.S. 63, 70, 175 U.S.P.Q. (BNA) 676 (1972). In other words, claims that require some kind of transformation of subject matter, which has been held to include intangible subject matter, such as data or signals, that are representative of or constitute physical activity or objects have been held to comply with Section 101. *See, for example, In re Warmerdam,* 31 U.S.P.Q.2d (BNA) 1754, 1759 n.5 (Fed. Cir. 1994) or *In re Schrader*, 22 F.3d 290, 295, 30 U.S.P.Q.2d (BNA) 1455, 1459 n.12 (Fed. Cir. 1994).

Thus, as expressly set forth in each of the independent claims, the claimed methods or system establish a bound based on a number of live frames, wherein the bound is a bound on the execution time of an application and transform a number of live frames of an application that are coexistent during execution of the application to a bound based on the number of live frames. This transformation to a bound based on the number of live frames provides a useful, concrete and tangible result.

Applicants submit that each of the claims 1-20 are in full compliance with 35 U.S.C. §101, and accordingly, respectfully request that the rejection under 35 U.S.C. §101 be withdrawn.

Section 112 Rejections

Claims 1-20 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. In particular, the Examiner asserts that it is unclear whether the "live frames" are related to the "instruction cache" because there is no connection made.

Applicants note that the present disclosure defines "live cache frames" as, for example, "a cache frame that contains a *block that is accessed in the future without an intervening eviction.* The present invention recognizes that the eviction of blocks from a live frame by an interrupt causes a future miss that would not otherwise occur and that evictions from live frames are the only evictions that cause misses that would not otherwise occur." (Page 2, lines 19-22; emphasis added.)

The "live frames" may be related to the "instruction cache;" this, however, is a design choice issue, as would be apparent to a person of ordinary skill in the art.

Thus, Applicants respectfully request that the section 112 rejections be withdrawn.

Independent Claims 1, 7, 13 and 16

Independent claims 1, 7, 13, and 16 were rejected under 35 U.S.C. §102(e) as being anticipated by Chilimbi et al. Regarding claim 1, the Examiner asserts that Chilimbi discloses determining a number of live frames of said application that are coexistent during execution of said application (determine active cache blocks) (col. 9, lines 1-21); and establishing said bound based on said number of live frames (cache block boundaries) (col. 8, lines 7-8).

Applicants note that the body of the cited claims require "establishing said bound," and that the preamble recites that the bound is "on the execution time of an application due to task interference in an instruction cache." Thus, since the preamble provides completeness for the body of the claims, the preamble should be given patentable weight and the established bound is a bound on the ***execution time of an application***. Chilimbi, however, does ***not*** address the issue of establishing a bound on the ***execution time of an application***, as required by the claims of the present invention, and does not disclose or suggest *establishing a bound, as defined in the present claims, based on the number of live frames.* Independent claims 1, 7, 13, and 16 require determining a number of live frames of said application that are

coexistent during execution of said application; and establishing said bound based on said number of live frames.

Thus, Chilimbi et al. do not disclose or suggest establishing said bound based on said number of live frames, as required by independent claims 1, 7, 13, and 16.

Dependent Claims 2-6, 8-12, 14-15 and 17-20

Dependent claims 2-6, 8-12, 14-15, and 17-20 were rejected under 35 U.S.C. §102(e) as being anticipated by Chilimbi et al.

Claims 2-6, 8-12, 14-15, and 17-20 are dependent on claims 1, 7, 13, and 16, respectively, and are therefore patentably distinguished over Chilimbi et al. because of their dependency from independent claims 1, 7, 13, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims, i.e., claims 1-20, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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